REMARKS

The enclosed is responsive to the Office Action mailed on May 30, 2006. At the time the Office Action was mailed, claims 18-37 were pending, with claims 25-37 withdrawn. By way of the present response the Applicant has amended no claims, added new claims 38-50, and canceled claims 25-37. As such, claims 18-24 and 38-50 remain pending. The Applicant respectfully requests reconsideration of the present application and the allowance of all claims presented.

Rejections under 35 U.S.C. 102(e)

The Office Action rejected claims 18-24 under 35 U.S.C. § 102(e) as being anticipated by *Farnworth*. The Applicant respectfully traverses. Farnworth does not disclose independent claim 18, which requires:

18. A stacked microelectronic device, comprising:
a first substrate of silicon, said first substrate having a top surface;
a first plurality of interconnect structures formed on at least a portion of the first substrate;
a layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate of silicon, at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures; and
a second substrate of silicon with a second plurality of interconnect structures formed thereon, said first and second substrates configured such that at least a portion of the interconnect structures of said first and second substrates respectively are in physical contact.

First, Farnworth does not disclose "a layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate", as required by claim 18. The Office Action asserts that Farnworth discloses this limitation by asserting that 71PGA of Figure 19G of Farnworth is "a layer of nonconductive compliant material" formed on at least a portion of the top surface of lower 16G in Figure 18A (the alleged "first substrate of silicon"). (*See* Office Action, p. 3.)

However, first, Farnworth does not disclose that 71G of Figure 19G is formed on at least a top surface of lower 16G of Figure 18A. In Farnworth, 71G is a dielectric layer that is part of component 16PGA. (*See* Farnworth, col. 30, lines 46-56 and Figure 19G.) Farnworth

does not describe that the dielectric layer 71G is formed on top of a component 16G. Farnworth excludes component 16PGA of Figure 19G from the listing of components described by component 16G of Figure 18A. Farnworth states: "In FIGS. 18A-18C a generic component 16G can comprise any one of the previously described components 16, 16EC, 16-5X, 16HS, 16A, 16A', 16A-A, 16A-B, 16A-C, 16A-D, 16I, 16E, 161-S, 16-1XHS or 16D. In addition, the generic component 16G can comprise the stacked system 83 of FIG. 10B." (Farnworth, col. 29, lines 56-64.) Farnworth does not describe that component 16PGA (shown in Figure 19G as including 71PGA, the alleged layer of nonconductive compliant material) is described by or equivalent to component 16G of Figure 18A. In Farnworth, component 16PGA is a separate embodiment. Farnworth states: "Referring to FIGS. 19A-19G and 20A-20F, steps in a method for fabricating a sixth embodiment semiconductor component 16PGA (FIG. 19G) are illustrated." (Farnworth, col. 30, lines 25-27, emphasis added.) Accordingly, Farnworth does not explicitly disclose that the alleged layer of nonconductive compliant material (71PGA of Figure 19G) is formed on at least a top surface of the alleged first substrate (lower 16G of Figure 18A).

Second, even if component 16PGA of Figure 19G is considered to be equivalent to component 16G of Figure 18A, Farnworth does not disclose that the dielectric layer 71PGA is formed on at least a top surface of that component (16PGA). Farnworth describes: "As shown in FIG. 19G, a singulated component 16PGA includes the thinned die 14T-PGA... In addition, the component 16PGA includes the circuit side polymer layer 36PGA". (Farnworth, col. 32, line 2-3, 10-11). As seen in Figure 19G, the dielectric layer 71PGA is between the die 14T-PGA and the polymer layer 36PGA, and inside the component 16PGA. In Farnworth, the dielectric layer 71PGA is not formed on at least a top surface of either the component 16PGA or the component 16G.

Therefore, Farnworth does not disclose or suggest "a layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate", as required by claim 18.

Additionally, Farnworth does not disclose or suggest "a first plurality of interconnect structures formed on at least a portion of the first substrate...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures".

The Office Action asserts that Farnworth discloses these limitations by equating terminals 42G of Figure 18A to the first plurality of interconnect structures of claim 18, pointing to the 71PGA just adjacent to 79PGA of Figure 19G of Farnworth, and citing col. 29, line 64 – col. 30, line 23. (*See* Office Action, p. 3.)

First, as discussed above, Farnworth discloses that the alleged layer of nonconductive compliant material 71PGA is inside the component 16PGA of Figure 19G. Farnworth does not disclose any particular relationship between the 71PGA of Figure 19G and the terminals 42G of Figure 18A. Therefore, Farnworth does not disclose "a first plurality of interconnect structures formed on at least a portion of the first substrate...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures", as asserted by the Office.

The Applicant respectfully submits that col. 29, line 64 – col. 30, line 23 of Farnworth also does not support the assertion that Farnworth discloses a first plurality of interconnect structures (allegedly 42G) formed on at least a portion of the first substrate...at least a portion of the layer of nonconductive compliant material (allegedly 71PGA) having a top surface lower than a top surface of at least one of said first plurality of interconnect structures (allegedly 42G). Col. 29, line 64 – col. 30, line 23 of Farnworth states:

> In FIG. 18A, a system in a package (SIP) 48 is constructed with one or more components 16G. This type of package is also referred to as a multi chip module MCM package. The system in a package (SIP) 48 can be configured to perform a desired function such as micro processing. The system in a package (SIP) 48 includes a substrate 52 having terminal leads 54. The components 16G can be flip chip mounted, or alternately edge connect mounted, to the substrate 52, with the terminal contacts 42G thereon in electrical communication with the terminal leads 54. The system in a package (SIP) 48 also includes a package body 56 encapsulating the components 16G and the substrate 52.
>
> Referring to FIGS. 18B and 18C, a multi chip module system 50 constructed with one or more components 16G is illustrated. The multi chip module system 50 includes a module substrate 58 having an edge connector 60, and a plurality of conductors 62 in electrical communication with the edge connector 60. The components 16G can be flip chip mounted, or alternately edge connect mounted, to the module substrate 58, with the terminal contacts 42 thereon in electrical communication with the conductors 62.
>
> One advantage of the system in a package (SIP) 48, and the multi chip module system 50, is that the components 16G have optionally been tested and burned-in at the wafer

level. If wafer level burn-in has been performed, the components have been certified as known good components (KGC). (Farnworth, col. 29, line 64 – col. 30, line 23, emphasis added.)

The cited section describes terminal contacts 42G on components 16G. The cited section does not describe 71PGA. The cited section does not disclose that at least a portion of the alleged nonconductive compliant material 71PGA has a top surface lower than a top surface of at least one of the alleged first plurality of interconnect structures 42G.

Therefore, Farnworth does not disclose the limitations of claim 18 of "a first plurality of interconnect structures formed on at least a portion of the first substrate...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures", as asserted by the Office.

Claim 18 is not anticipated by Farnworth. Claims 19-24 depend directly or indirectly from claim 18. Accordingly, for at least the reasons stated above, claims 19-24 are also patentable over Farnworth. Therefore, withdrawal of the rejection is respectfully requested.

New Claims

Farnworth also does not anticipate new claims 38-50.

New independent claims 38 and 45 each include limitations similar to those limitations of claim 18 specifically discussed above. Therefore, for at least the reasons discussed above, new independent claims 38 and 45 are each patentable over Farnworth. Additionally, new independent claims 38 and 45 each also recites "at least a portion of the interconnect structures of said first and second substrates respectively are in direct physical contact." Farnworth also does not disclose or suggest this limitation.

Farnworth describes: "The components 16G can be flip chip mounted, or alternately edge connect mounted, to the substrate 52, with the terminal contacts 42G thereon in electrical communication with the terminal leads 54. The system in a package (SIP) 48 also includes a package body 56 encapsulating the components 16G and the substrate 52." (Farnworth, col. 30, lines 3-6.) As the Office Action suggested, the terminal contacts 42G are in physical contact through substrate 52. (Office Action, p. 3, emphasis added.)

Farnworth does not describe that "at least a portion of the interconnect structures of said first and second substrates respectively are in direct physical contact", as required by each of claims 38 and 45. Therefore, for at least this additional reason, new independent claims 38 and 45 are each patentable over Farnworth.

Furthermore, new independent claim 45 also includes the limitation of "the layer of nonconductive compliant material structurally supporting the stacked substrates". Farnworth also does not disclose or suggest this limitation.

Farnworth describes that the dielectric layer 71PGA (the alleged layer of nonconductive compliant material) electrically insulates the die contacts 18PGA from the bulk of the substrate 14PGA, and from the integrated circuits on the substrate 14PGA. (Farnworth, col. 30, lines 47-50.) Farnworth describes that the dielectric layer 71PGA can comprise an electrically insulating material such as silicon dioxide, or polyimide, formed during fabrication of the wafer 12PGA. In addition, the dielectric layer 71PGA rather than being blanket deposited, can be located or can have a shape (e.g., donut shape) that insulates only selected portions of the substrate 14PGA.

Farnworth does not describe "the layer of nonconductive compliant material structurally supporting the stacked substrates", as required by each of claim 45. Therefore, for at least this additional reason, new independent claim 45 is further patentable over Farnworth.

Claims 39-44 and 46-50 each depend directly or indirectly from claim 38 or claim 45. Therefore, claims 39-44 and 46-50 are each also patentable over Farnworth for at least the reasons discussed above.

CONCLUSION

The Applicant believes that the above remarks are fully responsive to the Office Action dated May 30, 2006.

The Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Ms. Van N. Nguy or Mr. Michael A. Bernadicou at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 8/30, 2006

Van N. Nguy
Reg. No. 55,851

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300